

Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) A data input device of a DDR SDRAM comprising:
a clock pulse generator for ~~receiving an internal clock, which operates in a write mode, and~~ outputting a data-in-strobe signal ~~that is a first control signal based on an internal clock in a write mode;~~
a first data buffer ~~an operation of which is~~ being directly controlled by the data-in-strobe signal from the clock pulse generator and having an output line, ~~of~~ which corresponds to a first global input/output line of the DDR SDRAM; and
a second data buffer ~~an operation of which is~~ being directly controlled by the data-in-strobe signal from the clock pulse generator and having an output line, ~~of~~ which corresponds to a second global input-output line of the DDR SDRAM;
a multiplexer for receiving a first data, a second data, and a multiplexer control signal and determining, based on the multiplexer control signal, whether the first data is to be outputted to the first or second data buffer and whether the second data is to be outputted to the first or second data buffer,
wherein if ~~a second~~ the multiplexer control signal is in a low level and the data-in-strobe signal is high, the first data is directly applied to the first data buffer to be transferred to the first global input/output line, and second data is directly

applied to the second data buffer to be transferred to the second global input/output line; and

wherein if the ~~second~~ multiplexer control signal is in a high level and the data-in-strobe signal is high, the first data is directly applied to the second data buffer to be transferred to the second global input/output line, and the second data is directly applied to the first data buffer to be transferred to the first global input/output line.

2. (currently amended) The data input device of claim 1, wherein the ~~second~~ multiplexer control signal outputs a low level if the least significant bit (LSB) of a column address applied in the write mode is "0", and outputs a high level if the LSB of the column address applied in the write mode is "1".

3. (currently amended) The data input device of ~~claim 1~~ claim 5, wherein the first data buffer has only one data input terminal and selectively receives the first data or the second data through ~~one~~ the data input terminal controlled directly by the data-in-strobe signal.

4. (currently amended) The data input device of ~~claim 1~~ claim 5, wherein the ~~first~~ second data buffer has only one data input terminal and selectively receives the first data or the second data through the data input terminal controlled directly by the data-in-strobe signal ~~two input terminals~~.

5. (new) The data input device of claim 1, wherein the first data corresponds to 0 to even numbered data bursts from a sequence of data bursts, and wherein

the second data corresponds to 1 to odd numbered data bursts from a sequence of data bursts.

Amendments To The Drawings:

The attached sheets of drawings include changes to FIG. 8. These sheets contain corrections shown in red for the Examiner's approval and are requested to replace the original sheets of FIGS. 8.

Attachment: Replacement Sheet of FIG. 8.

Annotated Sheet Showing Change of FIG 8 in red.